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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/731,788	12/08/2000	Hiroshi Sukegawa	200714US2	1444

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EXAMINER	
GOSSAGE, GLENN A	
ART UNIT	**PAPER NUMBER**
2187	17

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/731,788	SUKEGAWA, HIROSHI	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,8,9,13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *1,4,6,8,9,13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *16*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. A Request for Continued Examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 26, 2004 has been entered.

2. In the title of the invention, as amended in the response filed February 26, 2004, "OUTPTTING" should be changed to --OUTPUTTING-- for clarity.

3. The proposed substitute sheets of drawings filed on February 26, 2004 have been approved by the Examiner, subject to drafting review.

4. It is once again noted that this application appears to contain claims directed to different inventions or different species of the same invention (here, an electrically rewritable nonvolatile semiconductor memory device). More specifically, the application contains claims (see claims 1, 4-6, 8, 15 and 18, e.g.) directed to an electrically rewritable nonvolatile semiconductor memory device including control circuits for sequentially controlling writing and, in various embodiments, a chip enable terminal or an inputted command for controlling the inactivity and inactivity of the memory circuits. Other claims (see claims 9, 13, 16-17 and 19-20, e.g.) are directed to an electrically rewritable nonvolatile

semiconductor memory device including plural memory circuits, each having at least one stage of a data buffer, writing operations being simultaneously carried out via the data buffer, and in which pass/fail results are outputted or accumulated.

While these inventions or species appear to be distinct, a restriction requirement is NOT being made at this time since it does not appear there will be a substantial burden on the Office if restriction is not required. However, restriction may be required in the future depending on how the claims are amended.

5. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

In the paragraph beginning on page 7, line 35 (as shown in the amendment filed February 26, 2004), at lines 2-3 of the paragraph, it is not clear what is meant by (is not) "controlled continuously" in this context, particularly when read in light of the language of the specification as originally filed ("a little control continues to enter each of the EEPROM circuits"). It appears "each EEPROM circuit is controlled continuously" should be changed to --control is continued for each EEPROM circuit-- for clarity, and to avoid possible questions of new matter.

In the paragraph beginning on page 9, line 11(as shown in the amendment filed February 26, 2004), at lines 8-9 of the paragraph, the language "Each of the EEPROM circuits 2 does not include controllers of command, address, and data" is somewhat unclear and confusing, particularly when read in light of the language of the specification as originally filed. It appears "controllers of command, address, and data" should be changed to --a control circuit, as do the EEPROM circuits 2 in the embodiments of Figures 1, 3, 5 and 6-- for clarity, and to avoid any possible questions of new matter.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claims 1 and 5, it appears "has" in line 3 should be changed to --having--, and "are" in line 5 changed to --being-- for clarity. [Otherwise, it appears --wherein-- should be inserted before "each" in line 3.]

In claim 9, line 2, it appears "comprising a" should be --comprising: a-- (i.e., a colon should be added and a new sub-paragraph started similar to claim 1, lines 2-3) for clarity and consistency. Note the changes made in claim 5, line 2, for example.

In claim 13, lines 10 and 12, it appears "said" should be changed to --its -- for clarity. Also in line 10, it appears "the" reads more clearly here as --that--. Similarly, in line 13, it appears "said" should be changed to --that memory circuit's-- for clarity and consistency (see lines 10-11, e.g.).

Appropriate correction is required.

6. Claims 1, 4, 6, 8, 13 and 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, and therefore its dependent claims, it is not entirely clear to what a "logical output of a signal of said master chip enable terminal" refers here, or how the activity and inactivity of each of the memory circuits is controlled by a "logical output" of the master chip enable terminal, i.e., the dependence of the "logical output" on the chip enable terminals is not clear (again compare the language of original claim 3, lines 4-7, e.g.). The language "logical output of a signal of said master chip enable terminal" is particularly unclear when read in conjunction with claim 4, lines 2-3. [Should language such as --and a respective chip enable terminal-- be inserted after "terminal" in line 10?]

In claim 6, and therefore claim 8 dependent therefrom, it is not entirely clear to what the "common chip enable terminal" refers here, i.e., how it is connected or related to the "master chip enable terminal" set forth in claim 5. [Should "a

common ... circuits, and" in lines 2-3 be deleted, and "common" in line 3 changed to --master--?]

In claim 13, and therefore its dependent claims, it is not entirely clear to where the at least one data buffer stage "transmits" the data (see line 4, e.g.). It appears "transmitting" in line 4 should be changed to --storing-- for clarity and consistency (note the changes made in claim 9, line 4, e.g.).

In claims 15-17, it remains unclear how the "memory circuits (have) a stacked gate structure." It appears "has" in claims 15-17, line 2 should be changed to --includes memory cells having-- for clarity and consistency (see page 4, line 30 of the original specification, e.g.).

Similarly, in claims 18-20, it is not clear how the "stacked gate structure (of the memory circuits) is a stacked gate structure." It appears "stacked gate structure is" in claims 18-20, line 2 should be changed to --memory cells are arranged in-- for clarity and consistency (in conjunction with the changes suggested above for claims 15-17. Note page 4, lines 30-31 of the original specification, e.g.).

[It is believed the changes with respect to claims 15-17 and 18-20 were discussed in the personal interview of December 6, 2003.]

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9 and 16, insofar as definite and clear, are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al.

The broad nature of the claim language is such that the claims "read on" a device disclosed by Lee et al, and thus are seen to be anticipated by Lee et al.

More specifically, with respect to claim 9, Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device such as an electrically erasable programmable read only memory (EEPROM) including a plurality of "memory circuits," provided in a memory chip, as in the present invention [see the EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 3, lines 15-17 and 55-58, e.g.]. Lee et al discloses that each of the memory circuits is provided with at least one 'stage' of a "data buffer" [see data registers 404, 405, 409 and 410 in Figure 3 and column 4, lines 46-49, e.g.] for transmitting or storing writing data corresponding to the address, and also teaches that writing operations in the plurality of memory circuits may be simultaneously carried out "via" or using the data buffer in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al also discloses that the "pass/fail" results of each of the writing operations may be ascertained by corresponding program/verify circuits (such as 454 and 460 in Figure 3, which may be considered to be a part of the data buffer 'stage') and outputted to each of the respective memory circuits. Lee et al

teaches that each of the data registers stores up to a chunk of data for a corresponding memory circuit (see column 4, lines 46-49, e.g.) and that a series of program/verify steps are performed until all bits of the data chunks are verified as having been programmed correctly (see column 5, lines 4-7, e.g.). Since a series of verify steps needs to be performed for bits in a data "chunk" before verifying that a particular data "chunk" has been correctly programmed, the pass/fail results for each of the writing operations for different bits in a data chunk may be considered to be "accumulated" in the data buffer 'stage.'

With respect to claim 16, the memory cells in Lee et al use nonvolatile EEPROM transistors which have a "stacked gate" (floating gate and control gate) structure.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al and Sukegawa et al, taken together.

Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits which may be simultaneously written in which "pass/fail" results of each of the writing

operations may be ascertained and "accumulated" by corresponding program/verify circuits. Lee et al also teaches that the memory circuits comprise nonvolatile EEPROM transistors which have a "stacked gate" (floating gate and control gate) structure, but does not explicitly using memory cells arranged or connected in a NAND structure.

However, the use of a NAND type structure in a nonvolatile memory such as an EEPROM was known in the art at the time the claimed invention was made. Sukegawa et al (U.S. '001), by way of example only, teaches using memory cells arranged in a NAND structure (see column 14, lines 28-30 and 52-54, e.g.). As one of ordinary skill in the art would readily appreciate, NAND type flash memories provide improved density and thus greater capacity memory in a smaller size since the number of interconnections or contacts between cells is reduced.

Accordingly, it would have been readily obvious to one of ordinary skill in the art a the time the claimed invention utilize a well known NAND type flash memory structure as taught by Sukegawa et al (U.S. '001) in conjunction with the nonvolatile EEPROM of Lee et al, in order to obtain a high capacity memory in which writing operations in a plurality of memory circuits may be simultaneously carried out, thereby resulting in a high speed memory device within a smaller circuit area.

9. Applicants' arguments filed February 26, 2004 have been considered but are not entirely persuasive, particularly with respect to the 35 U.S.C. 112, second paragraph, rejections and the rejection of claim 9 and its dependent claims based on prior art. It is believed applicants' arguments have been addressed in the preceding paragraphs.

With respect to claims 1 and 5, and their respective dependent claims, applicant's arguments are persuasive and the prior art rejections of these claims has been withdrawn.

10. Claim 5 is allowed over the prior art of record.

Claims 1, 4, 15 and 18, insofar as definite and clear, would appear to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 6, 8, 13, 17 and 20 would also appear to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187